Konami SCC K051649

5 channel wave table synhesizer

Features:
- 5 channels
- 12 bit frequency and 4 bit volume contro
- 11 bit sound output data
- 4x 32 byte wave table, one shared between ch. 4/5
- 8K rom mapper

The Konaimi SCC sound synthesizer IC is a chip that can produce up to 5 channels of independent sound. It has 5x 32 bytes wavetables per channel. One table is shared between channel 4 and 5.

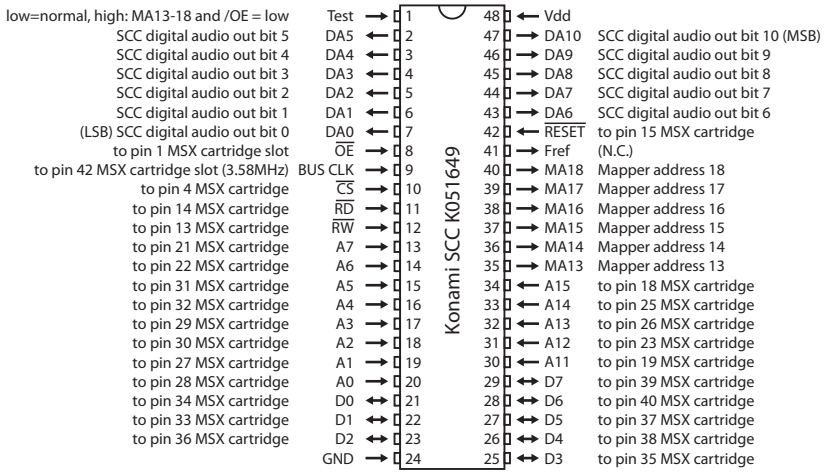
The SCC interfaces with an 8 bit data bus and 16 bit address bus of which lines A8-10 are unused.
It has a build-in memory mapper for the roms the cartridge supports.

When used for the intended system, a Z80 CPU environment with slot selection, ie in an MSX system, the chip enable pin is connected to the slot selector. When using the SCC directly, one can use the CS pin to enable the functionality.

Per channel there are 4 functions:
1. 32 bytes wave form
2. 12 bits frequency control
3. 4 bits volume control
4. 1 bit on/off switch

For timing and sound generation it uses a clock frequency of 3.579545 MHz.

An 11 bit DAC is needed in the form of a resistor ladder R2R.



Register mapping

The registers are mapped to local address space of the Z80 microprocessor from 0x9800 to 0x98FF. We'll omit the MSB 0x98.

0x00 - 0x1F	Waveform ch. 1
0x20 - 0x3F	Waveform ch. 2
0x40 - 0x5F	Waveform ch. 3
0x60 - 0x7F	Waveform ch. 4 and 5
0x80 - 0x81	Frequency ch. 1
0x82 - 0x83	Frequency ch. 2
0x84 - 0x85	Frequency ch. 3
0x86 - 0x87	Frequency ch. 4
0x88 - 0x89	Frequency ch. 5
0x8A	Volume ch. 1
0x8B	Volume ch. 2
0x8C	Volume ch. 3
0x8D	Volume ch. 4
0x8E	Volume ch. 5
0x8F	on/off switch ch. 1-5
0xE0 - 0xFF	Test register

Sound generation

The waveform is made up of 32, signed (two's complement) bytes. The waveform represents the actual form of the tone the sound chip produces.
It's a looped play back from byte 0 to 31, and then again from 0 to 31, etc.
A value of 0 means no amplitude. From 1 to 127 results in an increasingly higher amplitude. From -1 to -128 (FFh to 80h) results in an increasingly higher negative amplitude.

The frequency is stored and calculated the same way as in the PSG. The first byte contains bits 0 to 7 from the frequency. Bits 0 to 3 of the second byte contain bits 8 to 11 of the frequency. Bits 4 to 7 of the second byte are ignored. Remember that the value you enter is a period: a higher value gives a lower frequency.

$$ftone = \frac{fclock}{32 \times (time\ period + 1)}$$

fclock is the clock frequency of the system: 3.579545 MHz.
ftone is the frequency of the channel in Hz.
Time period is the value from register frequency channel x.
Calculated with LSB byte + (256 x MSB byte)

Volume
bits 0..3 from registers 0x8A - 0x8E are used where 0 is silent and 15 is maximum volume.

Sources:
http://bifi.msxnet.org/msxnet/tech/scc
https://www.msx.org/wiki/Konami_SCC